Combinational Circuits

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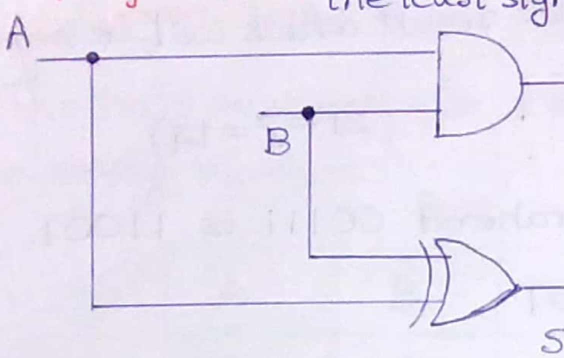
Half adder: When we add two binary numbers, we start with the least significant column. This circuit is called half adder.



CARRY = AB

↳ output of AND gate

↳ (high output when both inputs are high)

SUM = $\overline{A}B + A\overline{B}$

↳ output of exclusive OR gate

↓

(produces high output if either input, but not both is high)

A	B	CARRY	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

FULL ADDER

For higher order columns, we have to use Full Adder (a logic circuit that can add 3 bits at a time)

A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

C \ AB	00	01	11	10
0	0	0	1	0
1	0	1	1	1

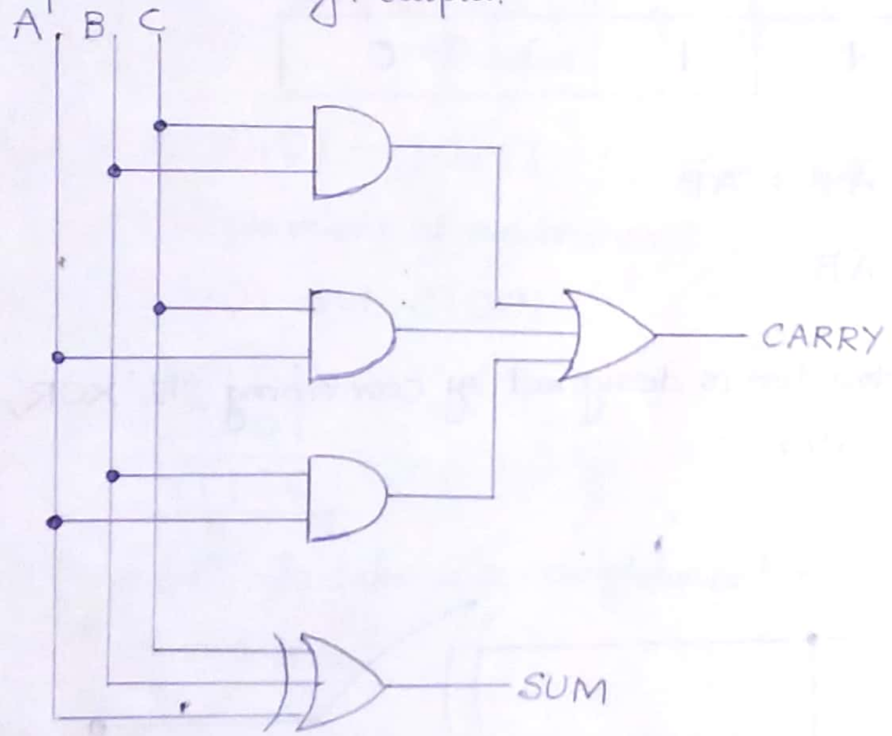
C \ AB	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$Carry = AB + BC + AC$

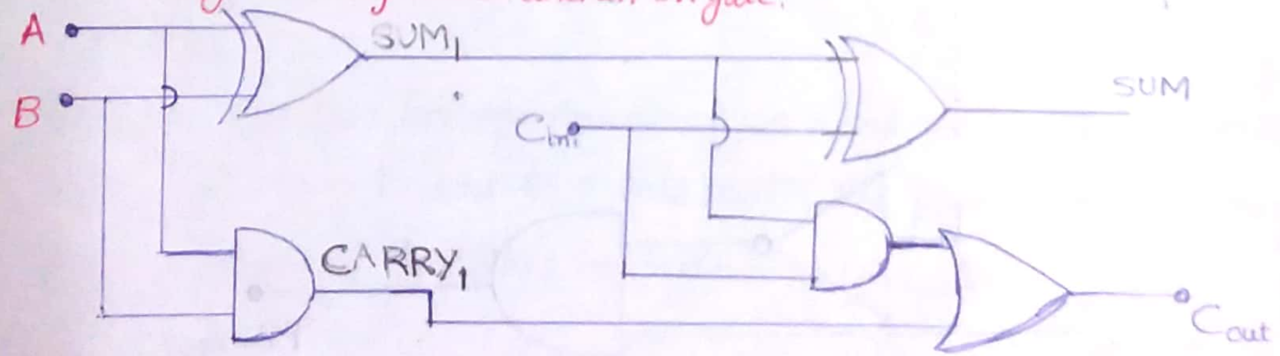
$SUM = A \oplus B \oplus C$

Carry is high when two or more of the ABC inputs are high.

When an odd number of high ABC inputs drives the exclusive OR-gate, it produces a high output.



Full adder by two half adder and an OR gate.



Half Subtractor :

The half subtractor is a ~~half~~ building block for subtracting two binary numbers.

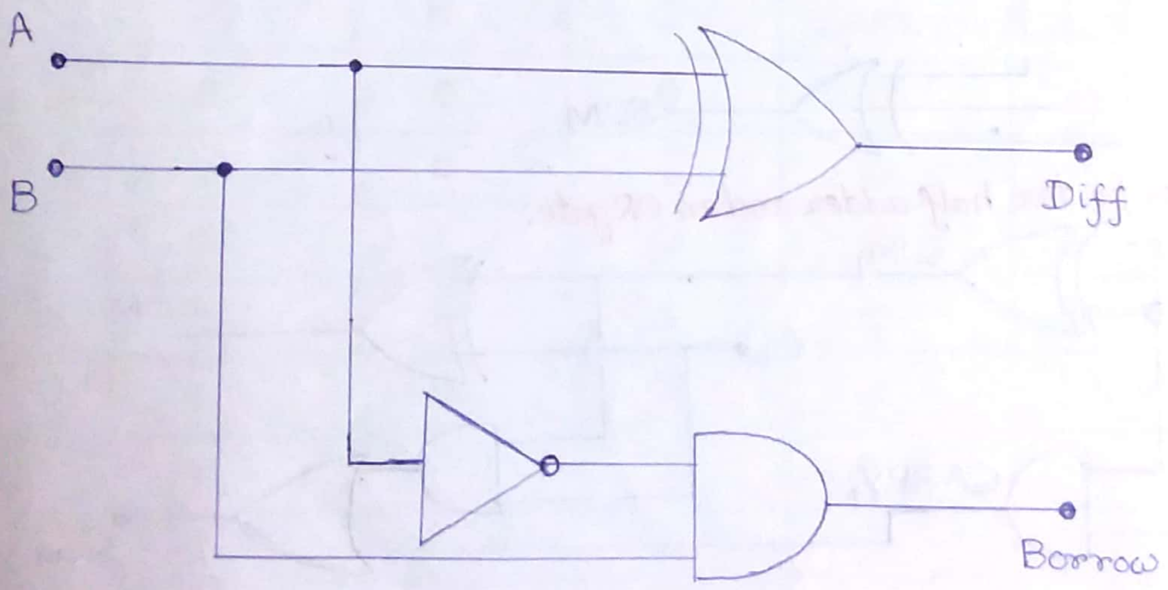
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$$Diff = \overline{A}B + A\overline{B}$$

$$Borrow = \overline{A}B$$

The half subtractor is designed by combining the 'XOR', 'AND' and 'NOT' gates.

Circuit



Full Subtractor

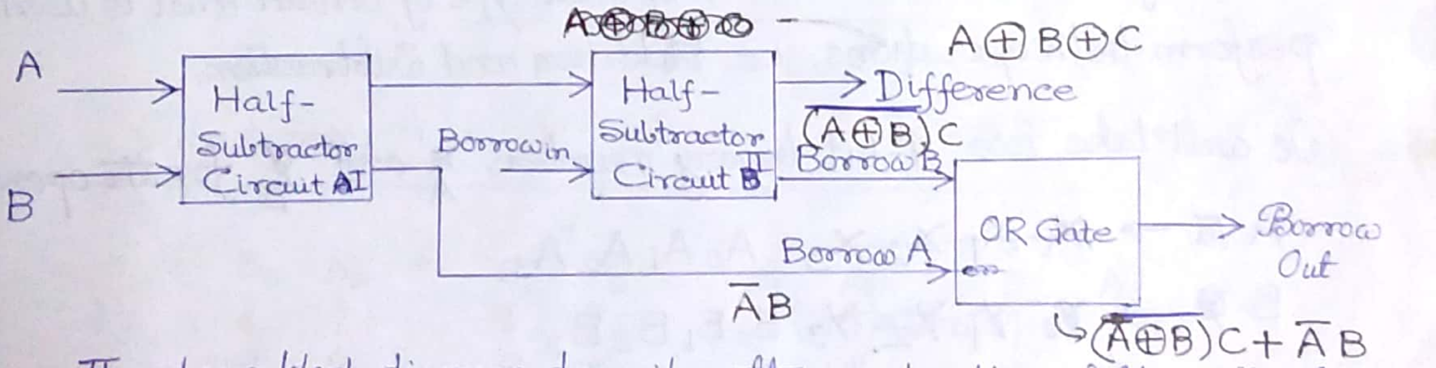
This is used to subtract three 1-bit numbers A, B and C, which minuend, subtrahend and borrow. It has two output states, diff and borrow.

Inputs			Output	
A	B	Borrow$_{in}$	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Borrow out

A \ BC	00	01	11	10
0	0	1	1	1
1	0	0	1	0

$\bar{A}C + BC + \bar{A}B$



The above block diagram describes the construction of the Full subtractor circuit.

There are two half adder circuits that are combined using the OR gate.

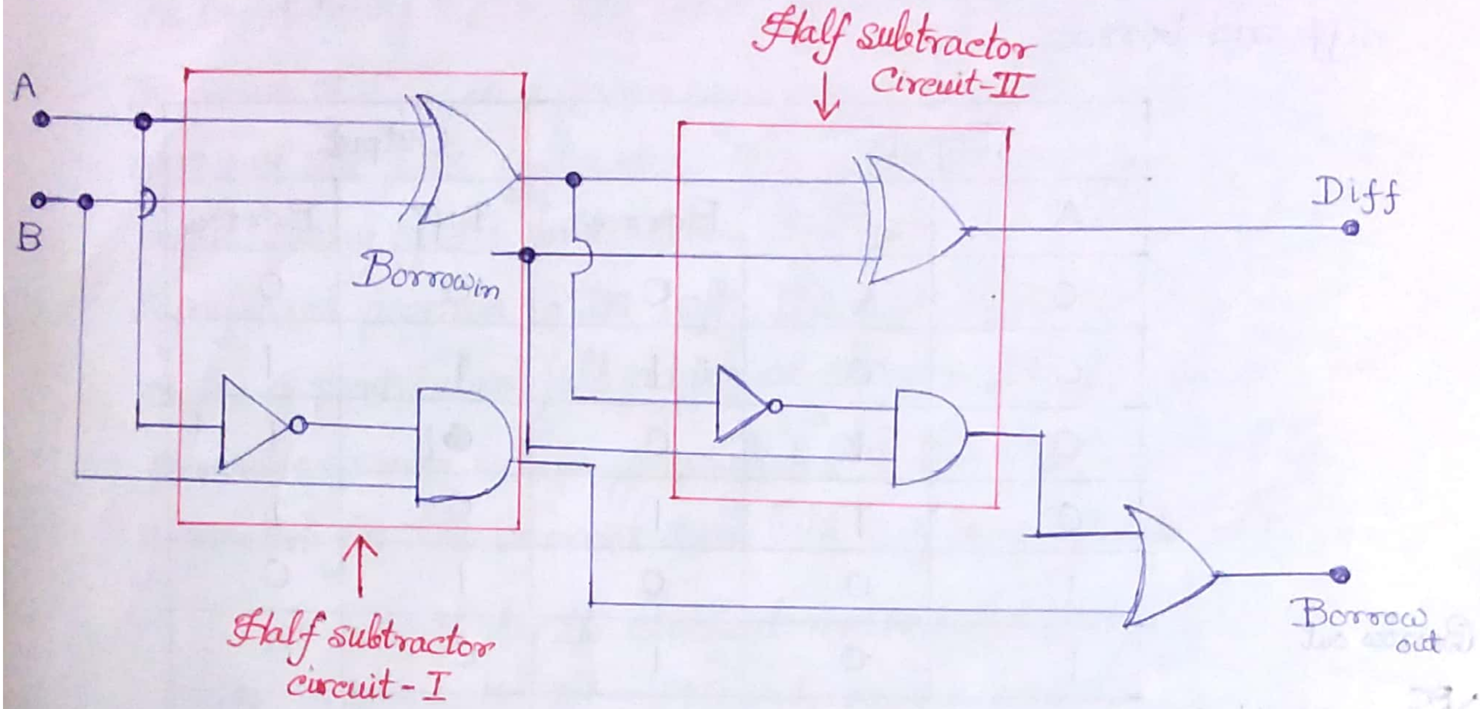
The first half subtractor has two inputs A and B and two outputs (Diff and Borrow). The 'Diff' output of the first subtractor will be the first input of the second half subtractor.

The "borrow$_{in}$" will be the second input of the second half subtractor.

The second half subtractor will again provide "Diff" and "Borrow".

The final outcome of the Full subtractor circuit is the "Diff" bit.

To find the final "Borrow" output, we provide the "Borrow" of the first and the second subtractor into the "OR" gate.



4-bit binary Adder/Subtractor

A binary Adder-Subtractor is a special type of circuit that is used to perform both operations, i.e. Addition and Subtraction.

We will take two 4-bit binary numbers 'A' and 'B' for the operation.

A → ~~X_0 X_1 X_2 X_3~~ $A_0\,A_1\,A_2\,A_3$

B → ~~Y_0 Y_1 Y_2 Y_3~~ $B_0\,B_1\,B_2\,B_3$

This circuit is a combination of 4 Full-adder, which is able to perform the addition and subtraction of 4-bit binary numbers. The control line determines whether the operation being performed is either subtraction or addition.

Binary Adder :

A binary adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascade, with the output carry from each full adder connected to the input carry of the next full adder in the chain.

Addition of n-bit numbers requires a chain of n full adders. The input carry to the least significant position is fixed at 0.

The augend bits of A and the addend bits of B are designated by subscript numbers from right to left, with subscript 0 denoting the least significant bit.

Subscript i:	3	2	1	0	
Input carry	0	1	1	0	← C_i
Augend	1	0	1	1	← A_i
Addend	0	0	1	1	← B_i
Sum	1	1	1	0	← S_i
Output carry	0	0	1	1	← C_{i+1}

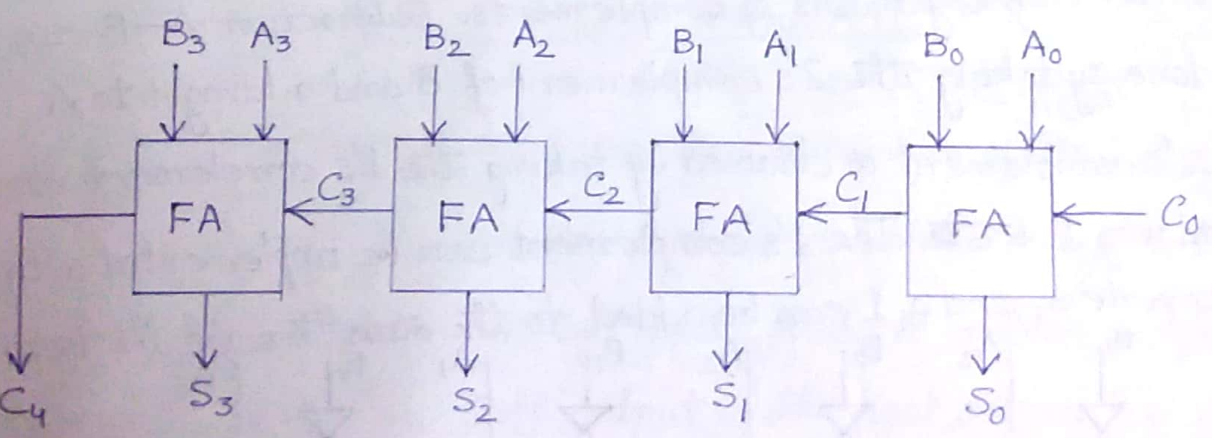


Fig. shows the inter-connection of four full adder (FA) circuits to provide a four-bit binary ripply carry adder. The carries are connected in a chain through the full adders. The S outputs generate the required sum bits.

DEL3-D

In our example, we have considered two binary numbers,

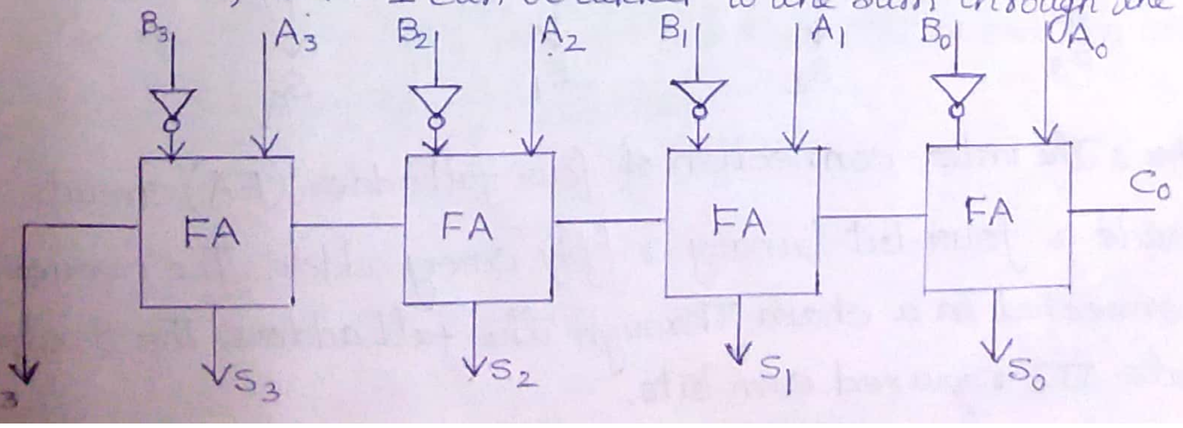
A = 1011 and B = 0011

The input carry C_0 in the least significant position must be 0. The value of C_{i+1} in a given significant position is the output carry of the i-th full adder. This value is transferred into the input carry of the next full adder that adds the bits one higher significant position to the left. The sum bits are thus generated for a particular full adder as soon as the corresponding previous carry bit is generated. All the carries must be generated for the correct sum bits to appear at the outputs.

In general by the classical method it would require a truth table with $2^9 = 512$ entries, since there are nine inputs to the circuit. By using an iterative method of cascading a standard function, it is possible to obtain a simple and straightforward implementation.

Binary Subtractor

The subtraction of unsigned binary numbers can be done most conveniently by means of complements. Subtraction A−B can be done by taking the 2's complement of B and adding it to A. 2's complement is obtained by taking the 1's complement and adding 1. The 1's complement can be implemented with inverters, and a 1 can be added to the sum through the input carry.



Let us take the example :

A → 1 0 1 1 $(11)_{10}$

B → 0 0 1 1 $(3)_{10}$

1's complement of B is 1100. Now add 1011 and 1100 with $C_0 = 1$

Here $C_0 = 1$

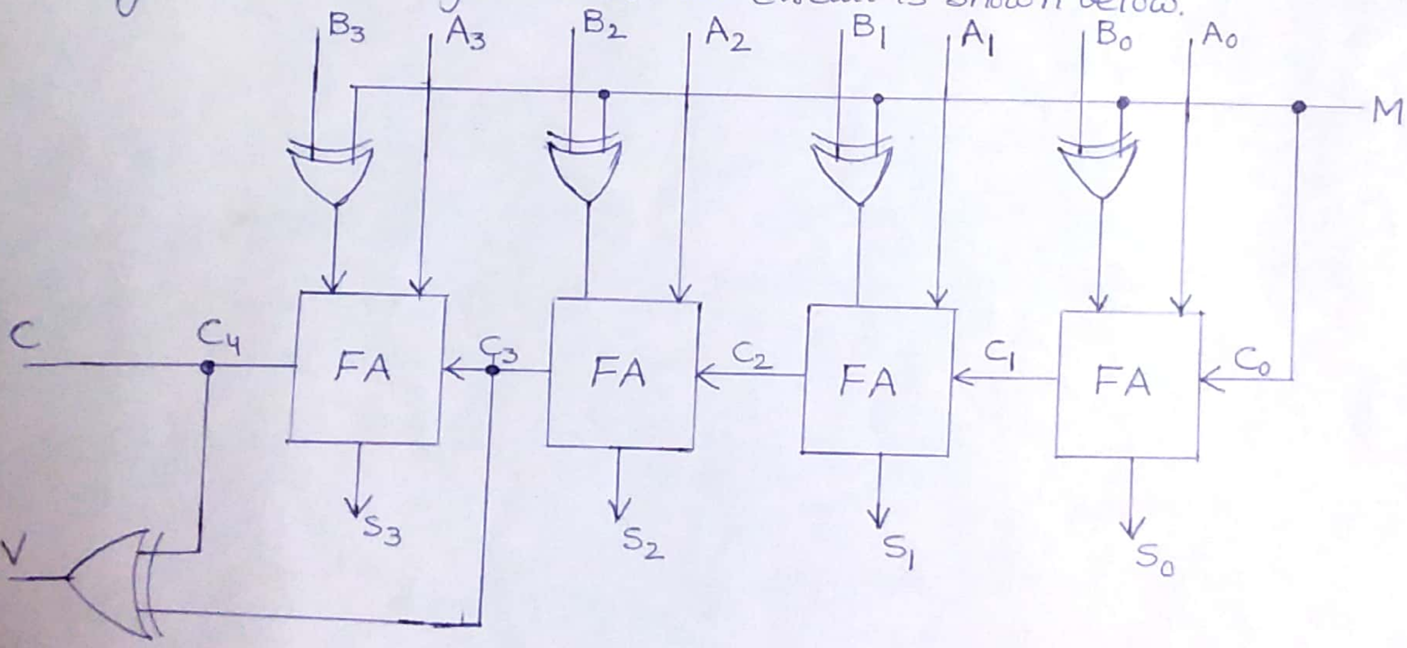
	C_3	C_2	C_1	C_0
	1	1	1	1
	1	0	1	1
	1	1	0	0
(1)	1	0	0	0

C_4 — C_4 is the final carry which is ignored

The final result is 1000 $(8)_{10}$

Binary adder - subtractor :

The addition and subtraction operations can be combined into one circuit with one common binary adder by including an exclusive-OR gate with each full adder. The circuit is shown below.



The mode input M controls the operation (adder/subtractor).

$M = 0 \longrightarrow$ adder

$= 1 \longrightarrow$ subtractor

· Each exclusive-OR gate receives input M and one of the inputs of B.

When $M = 0$, $B \oplus 0 = B \Rightarrow$ Full adders receive ~~the~~ value of B, ~~and the circuit~~ input carry is 0 and the circuit performs A plus B.

DEL4-B

When $M=1$, $B \oplus 1 = \overline{B}$ and $C_0=1$

As the B inputs are complemented and the input carry is 1, the circuit performs the operation "A plus 2's complement of B". (The exclusive-OR with output V is for detecting an overflow).